PAS6371LT CMOS VGA DIGITAL IMAGE SENSOR

General Description

The PAS6371LT is a highly integrated CMOS active-pixel image sensor that has a VGA YUV output of 640 x 480 pixels. It embedded the new FinePixel™ sensor technology to perform the excellent image quality. PAS6371LT outputs YUV/YCbCr 4:2:2 or RGB565/555/444 data through a parallel data bus. It is available in 29-pin CSP.

Features

- Resolution: 640 x 480 pixels
- Bayer-RGB color filter array
- Output format (8-bit):
  - YUV/YCbCr 4:2:2 (VGA, QVGA …)
  - RGB565/555/444 (VGA, QVGA …)
- On-chip 10-bit pipelined A/D converter
- On-chip 2-stage background compensation DAC
- Continuous variable frame time & exposure time
- I2C™ Interface
- Flash light timing
- Support 1.8V~3.3V I/O power
- 10uA low power-down dissipation ($V_{DD\text{-}A} = V_{DD\text{-}IO} = 2.8V$, $V_{DD\text{-}C} = 1.8V$)
- Automatic Background Compensation
- AEC & AGC function
- DSP function:
  - AWB
  - Gamma
  - Color matrix
  - Sharpness
  - De-noise
  - Color saturation
  - Defect compensation
  - Lens shading compensation
- WOI & Sub-sampling
- Critical Register table backward compatible with PAS6311

Key Specification

Resolution		640 (H) x 480 (V)
Power	Analog	2.5V ~ 3.0V
	I/O	1.8V ~ 3.3V
	Core	1.8V
Pixel Size		4.5µmx4.5µm
Lens Chief Ray Angle		28degree
Frame rate		30fps, VGA YUV mode
Max. System clock		48MHz
Max. Pixel clock		24MHz, VGA YUV mode
Sensitivity		2.1V/(Lux*Sec)
Color filter		RGB Bayer Pattern
Exposure Time		~ Frame time to Line time
Scan Mode		Progressive
S/N Ratio		41dB
Dynamic range		60dB
Package		29-pin CSP

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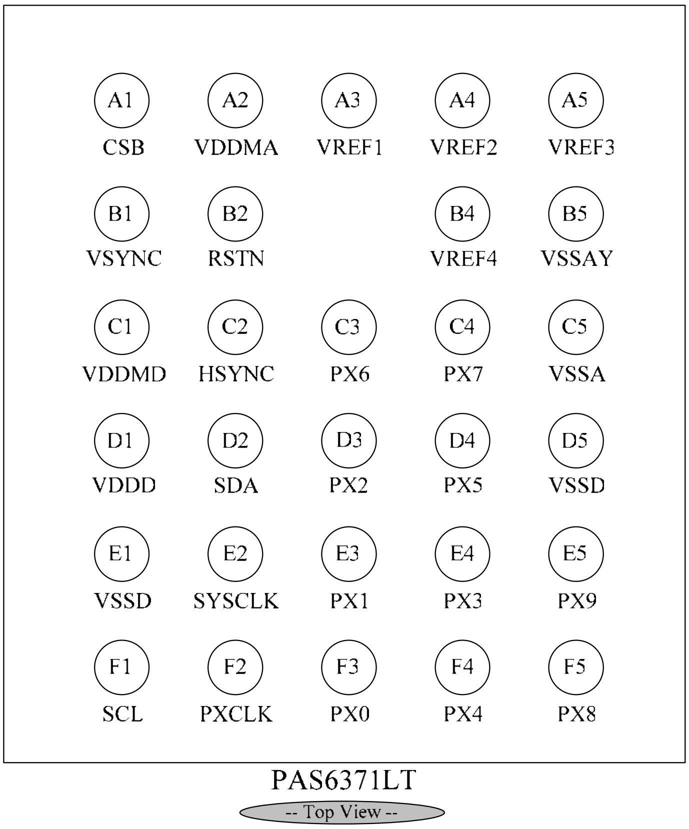
1. Pin Assignment



Pin No.	Name	Type	Description
A1	CSB	IN	Power down enable, active high
A2	VDDMA	PWR	Analog power, 2.5V ~ 3.0V
A3	VREF1	Ref	Internal voltage reference
A4	VREF2	Ref	Internal voltage reference
A5	VREF3	Ref	Internal voltage reference
B1	VSYNC	OUT	Vertical synchronization signal output
B2	RSTN	IN	Reset mode enable, active low
B4	VREF4	Ref	Internal voltage reference
B5	VSSAY	GND	Sensor array ground
C1	VDDMD	PWR	I/O power, 1.8V ~ 3.3V
C2	HSYNC	OUT	Horizontal synchronization signal output
C3	PX6	OUT	Digital data output
C4	PX7	OUT	Digital data output
C5	VSSA	GND	Analog ground
D1	VDDD	PWR	Digital core power, 1.8V
D2	SDA	I/O	I2C data
D3	PX2	OUT	Digital data output
D4	PX5	OUT	Digital data output
D5	VSSD	GND	Digital ground
E1	VSSD	GND	Digital ground

E2	SYSCLK	IN	External clock input
E3	PX1	OUT	Digital data output
E4	PX3	OUT	Digital data output
E5	PX9	OUT	Digital data output
F1	SCL	IN	I2C clock input
F2	PXCLK	OUT	Pixel clock output
F3	PX0	OUT	Digital data output
F4	PX4	OUT	Digital data output
F5	PX8	OUT	Digital data output

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2. Specifications

Absolute Maximum Ratings

Ambient Storage Temperature		-25℃~125℃
Supply Voltage (with respect to ground)	V_{DDD}	3.0V
	V_{DDMA}	4.5V
	V_{DDMD}	4.5V
All Input / Output Voltage (with respect to ground)		-0.3V to VDDMD+0.5V
Lead-free temperature, Surface-mount process		245℃
ESD rating, Human Body model		2000V

DC Electrical Characteristics (Ta = 0℃ ~ 70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Type : POWER					
V_{DDMA}	DC supply voltage – Analog	2.5	2.8	3.0	V
V_{DDD}	DC supply voltage – Digital core	1.62	1.8	1.98	V
V_{DDMD}	DC supply voltage – I/O	1.62		3.3	V
I_{DD}	Operating Current (see Note[a])		29		mA
I_{PWDN}	Power Down Current (see Note[b])		10	20	µA
Type : IN & I/O Reset and System Clock(input clock)					
V_{IH}	Input Voltage HIGH	VDDMD * 0.7			V
V_{IL}	Input Voltage LOW			VDDMD * 0.3	V
Type : OUT & I/O for PX0 : 9, SDA, H/VSYNC and PXCLK(output clock)					
V_{OH}	Output Voltage HIGH	VDDMD * 0.9			V
V_{OL}	Output Voltage LOW			VDDMD * 0.1	V

Note[a]: VDDMA=2.8V, VDDD=1.8V, VDDMD=3.3V, 30fps VGA YUV output, without I/O loading

Note[b]: VDDMA=2.8V, VDDMD=3.3V

AC Operating Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{sysclk}	System clock frequency		24		MHz
t_{sysclk_dc}	System clock duty cycle	45		55	%

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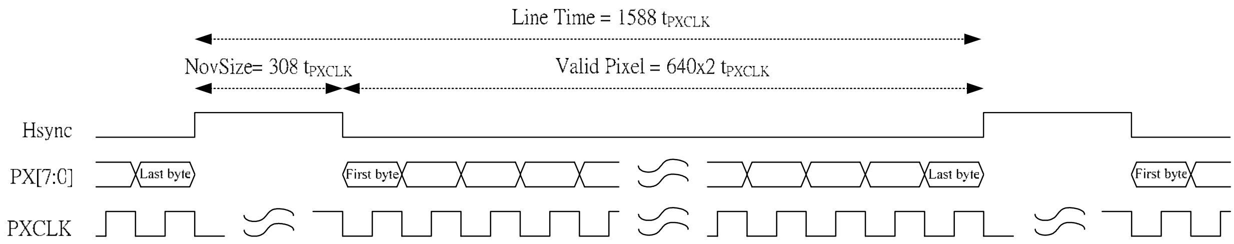
Sensor Characteristics

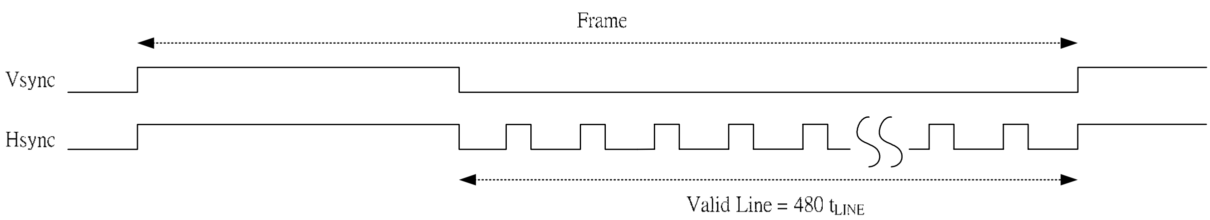
Parameter	Typ.	Unit
Sensitivity	2.1	V/Lux-sec
Signal to Noise Ratio	41	dB
Dynamic Range	60	dB

3. Output timing

VGA YUV output timing



Inter-line timing



Inter-frame timing

4. I2C™ Bus

PAS6371LT supports I2C bus transfer protocol and acts as slave device. The 7-bits unique slave address is "1000000" and supports receiving / transmitting speed as maximum 400KHz.

I2C Bus Overview

- Only two wires SDA (serial data) and SCL (serial clock) carry information between the devices connected to the I2C bus. Normally both SDA and SCL lines are open collector structure and pulled high by external pull-up resistors.
- Only the master can initiates a transfer (start), generates clock signals, and terminates a transfer (stop).
- Start and stop condition : A high to low transition of the SDA line while SCL is high defines a start condition. A low to high transition of the SDA line while SCL is high defines a stop condition. Please refer to Figure 2.1.
- Valid data : The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read / Write control bit is the LSB of the first byte. Please refer to Figure 2.2.
- Both the master and slave can transmit and receive data from the bus.
- Acknowledge : The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

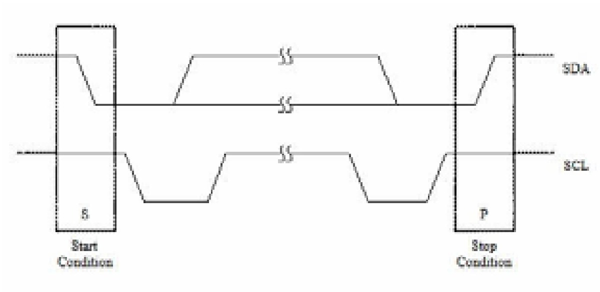


Figure 2.1 Start and Stop conditions

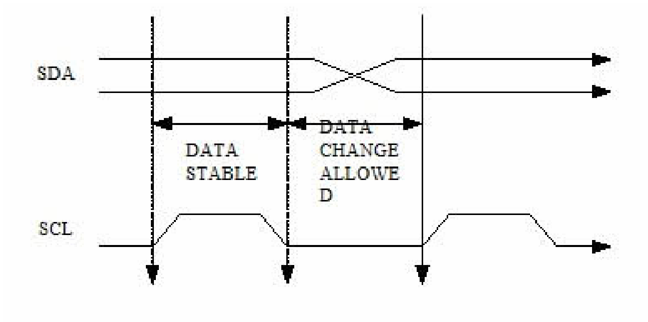
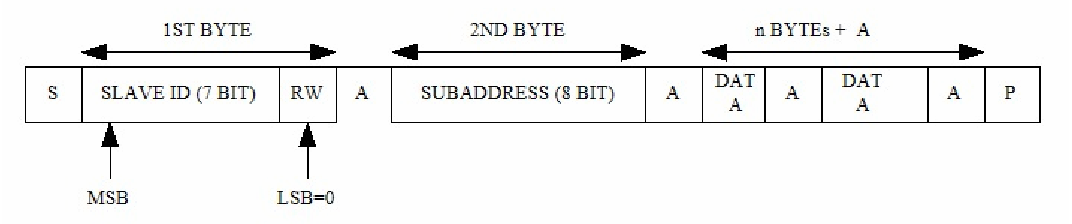


Figure 2.2 Valid Data

Data Transfer Format

Master transmits data to salve (write cycle)

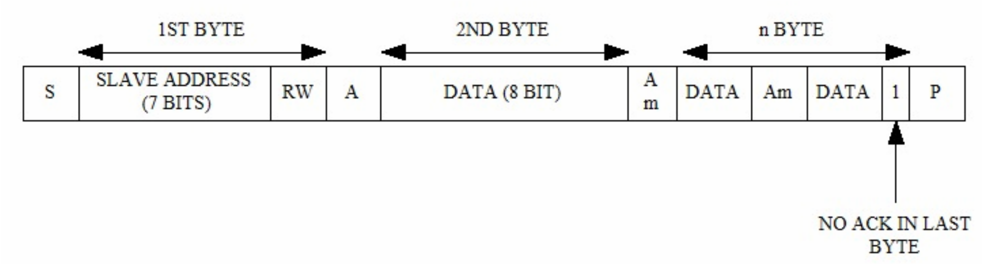
- S : Start.
- A : Acknowledge by salve.
- P : Stop.
- RW : The LSB of 1^{ST} byte to decide whether current cycle is read or write cycle. RW = 1 – Read cycle, RW = 0 – Write cycle.
- SUBADDRESS : The address values of PAS6371LT internal control registers. (Please refer to PAS6371LT register description)



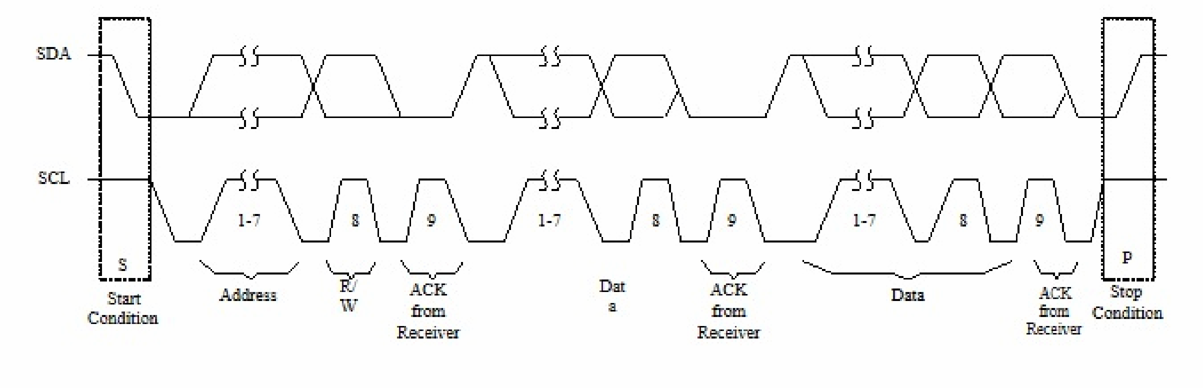
During write cycle, the master generates start condition and then places the 1^{st} byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After slave (PAS6371LT) issues acknowledgment, the master places 2^{nd} byte (Sub Address) data on SDA line. Again follow the PAS6371LT acknowledgment, the master places the 8 bits data on SDA line and transmit to PAS6371LT control register (address was assigned by 2^{nd} byte). After PAS6371LT issues acknowledgment, the master can generate a stop condition to end of this write cycle. In the condition of multi-byte write, the PAS6371LT sub-address is automatically increment after each DATA byte transferred. The data and A cycles is repeat until last byte write. Every control registers value inside PAS6371LT can be programming via this way.

Slave transmits data to master (read cycle)

- The sub-address was taken from previous write cycle.
- The sub-address is automatically increment after each byte read.
- Am : Acknowledge by master.
- Note there is no acknowledgment from master after last byte read.



During read cycle, the master generates start condition and then place the 1^{st} byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After issue acknowledgment, 8 bits DATA was also placed on SDA line by PAS6371LT. The 8 bits data was read from PAS6371LT internal control register that address was assigned by previous write cycle. Follow the master acknowledgment, the PAS6371LT place the next 8 bits data (address is increment automatically) on SDA line and then transmit to master serially. The DATA and Am cycles is repeat until the last byte read. After last byte read, Am is no longer generated by master but instead by keep SDA line high. The slave (PAS6371LT) must releases SDA line to master to generate STOP condition.



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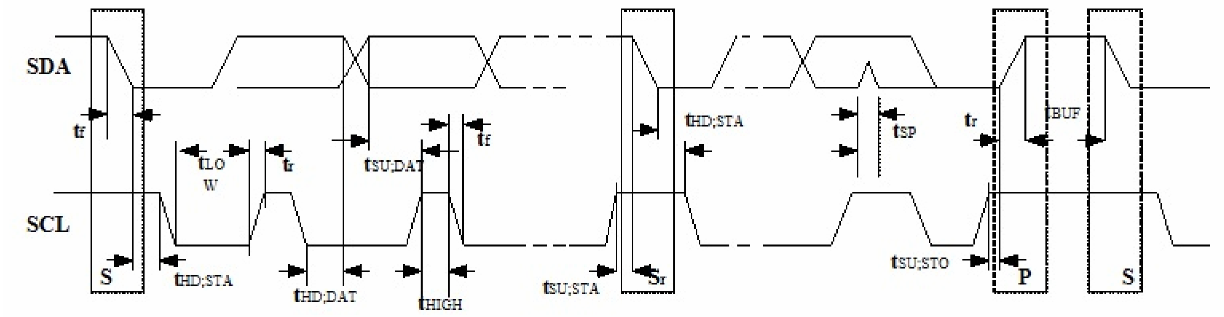
I2C™ Bus Timing



I2C™ Bus Timing Specification

Parameter	Symbol	Standard Mode		Unit
		Min.	Max	
SCL clock frequency.	f_{scl}	10	400	KHz
Hold time (repeated) Start condition. After this period, the first clock pulse is generated.	$t_{HD:STA}$	4.0	-	μs
Low period of the SCL clock.	t_{LOW}	4.7	-	μs
High period of the SCL clock.	t_{HIGH}	0.75	-	μs
Set-up time for a repeated START condition.	$t_{SU;STA}$	4.7	-	μs
Data hold time. For I2C-bus device.	$t_{HD;DAT}$	0	3.45	μs
Data set-up time.	$t_{SU;DAT}$	250	-	ns
Rise time of both SDA and SCL signals.	t_r	30	N.D.	ns (notel)
Fall time of both SDA and SCL signals.	t_f	30	N.D.	ns (notel)
Set-up time for STOP condition.	$t_{SU;STO}$	4.0	-	μs
Bus free time between a STOP and START.	t_{BUF}	4.7	-	μs
Capacitive load for each bus line.	C_b	1	15	pF
Noise margin at LOW level for each connected device. (Including hysteresis)	V_{nL}	0.1 VDD	-	V
Noise margin at HIGH level for each connected device. (including hysteresis)	V_{nH}	0.2 VDD	-	V

Note : It depends on the “high” period time of SCL.

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5. Registers

Register Table

Bank0 (set address_0xEF=0)

Address (Hex)		Register name	Default	Description
-		I2C Slave ID for Write cycle	0x80	I2C Slave ID for Write cycle
-		I2C Slave ID for Read cycle	0x81	I2C Slave ID for Read cycle
00	[7:0]	PartID[15:8]	0x63	Part ID
01	[7:0]	PartID[7:0]	0x71	Part ID
02	[3:0]	VersionID[3:0]	0x00	VersionID
03	[7:0]	Reserved	xx	Reserved
04	[4:0]	AE_stage_indoor[4:0]	0x0c	Min. AE stage clamp in door
05	[7:0]	Reserved	0x01	Reserved
06	[0]	in_door	0x00	AE In door enable
07 - 0C	[7:0]	Reserved	0x00	Reserved
0D	[2:0]	AWB_RegionWeight_C[2:0]	0x01	Weighting of AWB region C
	[6:4]	AWB_RegionWeight_B[2:0]	0x01	Weighting of AWB region B
0E	[2:0]	AWB_RegionWeight_A[2:0]	0x01	Weighting of AWB region A
0F	[7:0]	AWB_Window_X[7:0]	0x90	AWB window width
10	[2:0]	AWB_Window_X[10:8]	0x01	AWB window width
11	[7:0]	AWB_Window_Y[7:0]	0x2c	AWB window height
12	[2:0]	AWB_Window_Y[10:8]	0x01	AWB window height
13 - 14	[7:0]	Reserved	xx	Reserved
15	[7:0]	AE_Window_X[7:0]	0x90	AE window width
16	[2:0]	AE_Window_X[10:8]	0x01	AE window width
17	[7:0]	AE_Window_Y[7:0]	0x2c	AE window height
18	[2:0]	AE_Window_Y[10:8]	0x01	AE window height
19 - 25	[7:0]	Reserved	xx	Reserved
26	[0]	CCMb_En	0x01	Color Correction Matrix enable (ISP_UpdateFlag=1, update)
27	[7:0]	CCMb0_0	0x4c	Color Correction Matrix coefficient unsigned 8bit, 2.6 format, 0~+4 (ISP_UpdateFlag=1, update)
28	[7:0]	CCMb0_1	0xf4	Color Correction Matrix coefficient signed 7bit, 1.6 format, -2~0~+2 (ISP_UpdateFlag=1, update)
29	[7:0]	CCMb0_2	0x00	Color Correction Matrix coefficient signed 7bit, 1.6 format, -2~0~+2 (ISP_UpdateFlag=1, update)
2A	[7:0]	CCMb1_0	0xf2	Color Correction Matrix coefficient signed 7bit, 1.6 format, -2~0~+2 (ISP_UpdateFlag=1, update)
2B	[7:0]	CCMb1_1	0x66	Color Correction Matrix coefficient unsigned 8bit, 2.6 format, 0~+4 (ISP_UpdateFlag=1, update)
2C	[7:0]	CCMb1_2	0xe8	Color Correction Matrix coefficient signed 7bit, 1.6 format, -2~0~+2 (ISP_UpdateFlag=1, update)

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2D	[7:0]	CCMb2_0	0x00	Color Correction Matrix coefficient signed 7bit, 1.6 format, -2~0~+2 (ISP_UpdateFlag=1, update)
2E	[7:0]	CCMb2_1	0xe6	Color Correction Matrix coefficient signed 7bit, 1.6 format, -2~0~+2 (ISP_UpdateFlag=1, update)
2F	[7:0]	CCMb2_2	0x5a	Color Correction Matrix coefficient unsigned 8bit, 2.6 format, 0~+4 (ISP_UpdateFlag=1, update)
34 - 4F	[7:0]	Reserved	xx	Reserved
50	[7:0]	CSM1_1	0xa7	Color saturation Matrix coefficient unsigned 8bit, 1.7 format, 0~+2
51	[7:0]	CSM0_0	0xc2	Color saturation Matrix coefficient unsigned 8bit, 1.7 format, 0~+2
52	[7:0]	CSM1_0	0x1c	Color saturation Matrix coefficient unsigned 8bit, 1.7 format, 0~+2
53	[7:0]	CSM2_2	0xd4	Color saturation Matrix coefficient unsigned 8bit, 1.7 format, 0~+2
54	[7:0]	CSM0_2	0x0b	Color saturation Matrix coefficient unsigned 8bit, 1.7 format, 0~+2
55	[7:0]	CSM0_1	0x38	Color saturation Matrix coefficient unsigned 8bit, 1.7 format, 0~+2
56	[7:0]	AG_stage_UB	0x3f	AG_stage upper bound at max AE_stage
57	[7:0]	Reserved	xx	Reserved
58	[7:0]	ISP_Y0	0x04	ISP Gamma Y0 (ISP_UpdateFlag=1, update)
59	[7:0]	ISP_Y1	0x08	ISP Gamma Y1 (ISP_UpdateFlag=1, update)
5A	[7:0]	ISP_Y2	0x10	ISP Gamma Y2 (ISP_UpdateFlag=1, update)
5B	[7:0]	ISP_Y3	0x20	ISP Gamma Y3 (ISP_UpdateFlag=1, update)
5C	[7:0]	ISP_Y4	0x32	ISP Gamma Y4 (ISP_UpdateFlag=1, update)
5D	[7:0]	ISP_Y5	0x44	ISP Gamma Y5 (ISP_UpdateFlag=1, update)
5E	[7:0]	ISP_Y6	0x71	ISP Gamma Y6 (ISP_UpdateFlag=1, update)
5F	[7:0]	ISP_Y7	0x90	ISP Gamma Y7 (ISP_UpdateFlag=1, update)
60	[7:0]	ISP_Y8	0xae	ISP Gamma Y8 (ISP_UpdateFlag=1, update)
61	[7:0]	ISP_Y9	0xca	ISP Gamma Y9 (ISP_UpdateFlag=1, update)
62	[0]	ISP_Gamma_EnH	0x00	ISP gamma correction enable (ISP_UpdateFlag=1, update)
63	[4]	ISP_EnH_update	0x00	Flag: ISP enable is sync by vsync
	[5]	ISP_EnH	0x01	ISP enable
64	[0]	saturation_En	0x01	Color saturation matrix enable

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	[1]	CSM_mode	0x01	1:HW Count CSMatrix(R2_x8a) 0:original
65	[7:0]	Reserved	xx	Reserved
66	[0]	freq_60	0x01	Set de-flicker frequency 0/1: 50/60Hz
	[4]	AE_EnH	0x01	AE enable
	[7:5]	Reserved	xx	Reserved
67	[7:0]	SysClk_freq[7:0]	0x97	Input_frequency / 2048
68	[6:0]	SysClk_freq[14:8]	0x31	Input_frequency / 2048
69 - 6A	[7:0]	Reserved	xx	Reserved
6B	[4:0]	AE_minStage[4:0]	0x01	Minimum AE stage
6C	[4:0]	AE_maxStage[4:0]	0x1c	Maximum AE stage (AE_maxStage<=28)
6D - 6E	[7:0]	Reserved	xx	Reserved
6F	[7:0]	Ytar8bit	0x64	0~255, Target luminance of AE
70	[2:0]	AE_wait_state	0x00	Frame wait-state for AE adjust
	[6:4]	AWB_wait_state	0x00	Frame wait-state for AWB adjust
71	[7:0]	Reserved	xx	Reserved
72	[0]	AWB_EnH	0x01	Auto-white balance enable
	[4]	AWB_Gain_rst	0x00	AWB gain gain reset
	[7:5]	Reserved	xx	Reserved
73 - 8A	[7:0]	Reserved	xx	Reserved
8B	[0]	AE_DeOsc_En	0x00	AE DeOscillate enable
	[1]	AE_DeOsc_Timer_En	0x00	AE DeOscillate escape timer enable
	[2]	AWB_DeOsc_En	0x00	AWB DeOscillate enable
	[3]	AWB_DeOsc_Timer_En	0x00	AWB DeOscillate escape timer enable
8D - 8E	[7:0]	Reserved	xx	Reserved
8F	[7:0]	ImgEffect_c0	0x40	Image Effect parameter 0 (ISP_UpdateFlag=1, update)
90	[7:0]	ImgEffect_c1	0x40	Image Effect parameter 1 (ISP_UpdateFlag=1, update)
91	[7:0]	ImgEffect_c2	0x10	Image Effect parameter 2 (ISP_UpdateFlag=1, update)
92	[7:0]	ImgEffect_c3	0x80	Image Effect parameter 3 (ISP_UpdateFlag=1, update)
93	[3:0]	ImgEffectMode	0x00	Image Effect mode 1: monochrome; 2: negative 3: Sepia; 4: Emboss; 5: Sketch 6: Black Board; 7: White Board 8: Solarize; 9: Color range R 10: Color range G; 11: Color range B; 12: Contrast (ISP_UpdateFlag=1, update)
	[5:4]	ImgEffectFilter	0x00	Image Effect emboss filter type (ISP_UpdateFlag=1, update)
94	[0]	ISP_ImgEffect_En	0x00	(ISP_UpdateFlag=1, update)
95 - 96	[7:0]	Reserved	xx	Reserved
97	[4]	Shading_EnH	0x00	Lens shading enable
	[5]	Shading_On	0x00	Shading on/off status
98	[0]	ShadingAutoOff	0x01	1:turn off shading
	[7:1]	Reserved	xx	Reserved

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99	[6:0]	BYcoef_D	0x1f	Y coefficient of color B
9A	[6:0]	BXcoef_R	0x1f	X coefficient of color B
9B	[6:0]	BYcoef_U	0x1f	Y coefficient of color B
9C	[6:0]	BXcoef_L	0x1f	X coefficient of color B
9D	[6:0]	GbYcoef_D	0x1f	Y coefficient of color Gb
9E	[6:0]	GbXcoef_R	0x1f	X coefficient of color Gb
9F	[6:0]	GbYcoef_U	0x1f	Y coefficient of color Gb
A0	[6:0]	GbXcoef_L	0x1f	X coefficient of color Gb
A1	[6:0]	GrYcoef_D	0x1f	Y coefficient of color Gr
A2	[6:0]	GrXcoef_R	0x1f	X coefficient of color Gr
A3	[6:0]	GrYcoef_U	0x1f	Y coefficient of color Gr
A4	[6:0]	GrXcoef_L	0x1f	X coefficient of color Gr
A5	[6:0]	RYcoef_D	0x1f	Y coefficient of color R
A6	[6:0]	RXcoef_R	0x1f	X coefficient of color R
A7	[6:0]	RYcoef_U	0x1f	Y coefficient of color R
A8	[6:0]	RXcoef_L	0x1f	X coefficient of color R
A9	[7:0]	brightestX[7:0]	0x40	brightest X
AA	[1:0]	brightestX[9:8]	0x01	brightest X
AB	[7:0]	brightestY[7:0]	0xf0	brightest Y
AC	[1:0]	brightestY[9:8]	0x00	brightest Y
B9	[2:0]	LensShfBit[2:0]	0x00	Lens Shift Bit select
BD - BE	[7:0]	Reserved	xx	Reserved
BF	[7:0]	Ycap8bit	0x00	Y sum report
C0	[5:0]	Reserved	xx	Reserved
	[6]	AWB_EnH_vs	0x00	AWB enable sync by vsync
	[7]	AE_EnH_vs	0x00	AE enable sync by vysnc
C1 - D4	[7:0]	Reserved	xx	Reserved
D7	[7:0]	ISP_HSize[7:0]	0xe0	ISP output Horizontal size (before skip function)
D8	[2:0]	ISP_HSize[10:8]	0x01	ISP output Horizontal size (before skip function)
D9	[7:0]	ISP_VSize[7:0]	0x68	ISP output Vertical size (before skip function)
DA	[2:0]	ISP_VSize[10:8]	0x01	ISP output Vertical size (before skip function)
DB – E6	[7:0]	Reserved	xx	Reserved
ED	[0]	ISP_Update		ISP_UpdateFlag
	[7:1]	Reserved	xx	Reserved
EE	[7:0]	Reserved	xx	Reserved

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Bank2 (set address_0xEF=2)

Address (Hex)		Register name	Default	Description
00	[0]	ISP2_Update	0x00	ISP2_UpdateFlag
01 - 03	[7:0]	Reserved	xx	Reserved
04	[7:0]	ImgEffect_R_Gain[7:0]	0x00	(ISP2_UpdateFlag=1, update)
05	[7:0]	ImgEffect_G_Gain[7:0]	0x00	(ISP2_UpdateFlag=1, update)
06	[7:0]	ImgEffect_B_Gain[7:0]	0x00	(ISP2_UpdateFlag=1, update)
07	[7:0]	ImgEffect_R_offset[7:0]	0x00	(ISP2_UpdateFlag=1, update)
08	[7:0]	ImgEffect_G_offset[7:0]	0x00	(ISP2_UpdateFlag=1, update)
09	[7:0]	ImgEffect_B_offset[7:0]	0x00	(ISP2_UpdateFlag=1, update)
0A	[0]	ISP_ImgEffect_1_En	0x00	(ISP2_UpdateFlag=1, update)
0E - 13	[7:0]	Reserved	xx	Reserved
17	[0]	Curve_EnH	0x01	ISP tone curve Enable
18	[7:0]	Curve_Y0[7:0]	0x1a	ISP tone curve Y0
19	[7:0]	Curve_Y1[7:0]	0x34	ISP tone curve Y1
1A	[7:0]	Curve_Y2[7:0]	0x49	ISP tone curve Y2
1B	[7:0]	Curve_Y3[7:0]	0x5b	ISP tone curve Y3
1C	[7:0]	Curve_Y4[7:0]	0x6d	ISP tone curve Y4
1D	[7:0]	Curve_Y5[7:0]	0x7d	ISP tone curve Y5
1E	[7:0]	Curve_Y6[7:0]	0x9a	ISP tone curve Y6
1F	[7:0]	Curve_Y7[7:0]	0xb6	ISP tone curve Y7
20	[7:0]	Curve_Y8[7:0]	0xcf	ISP tone curve Y8
21	[7:0]	Curve_Y9[7:0]	0xe8	ISP tone curve Y9
22	[3]	Defect_EnH	0x00	R_Defect_EnH
23 - 29	[7:0]	Reserved	xx	Reserved
2A	[6:0]	Reserved	xx	Reserved
	[7]	ISP_Edge_En0	0x01	ISP edge enhancement enable
2B - 69	[7:0]	Reserved	xx	Reserved
9B	[2:0]	ISP_WOI_HSize[10:8]	0x02	(ISP2_UpdateFlag=1, update)
	[4]	ISP_WOI_H_En	0x01	(ISP2_UpdateFlag=1, update)
9C	[7:0]	ISP_WOI_HSize[7:0]	0x80	(ISP2_UpdateFlag=1, update)
9D	[2:0]	ISP_WOI_VSize[10:8]	0x01	(ISP2_UpdateFlag=1, update)
	[4]	ISP_WOI_V_En	0x01	(ISP2_UpdateFlag=1, update)
9E	[7:0]	ISP_WOI_VSize[7:0]	0xE0	(ISP2_UpdateFlag=1, update)
9F	[2:0]	ISP_WOI_HOffset[10:8]	0x00	(ISP2_UpdateFlag=1, update)
A0	[7:0]	ISP_WOI_HOffset[7:0]	0x00	(ISP2_UpdateFlag=1, update)
A1	[2:0]	ISP_WOI_VOffset[10:8]	0x00	(ISP2_UpdateFlag=1, update)
A2	[7:0]	ISP_WOI_VOffset[7:0]	0x00	(ISP2_UpdateFlag=1, update)
A3 - B3	[7:0]	Reserved	xx	Reserved
B4	[2:0]	R_ISP_WOIb_HSize[10:8]	0x02	WOIb_HSize (ISP2_UpdateFlag=1, update)
B5	[7:0]	R_ISP_WOIb_HSize[7:0]	0x80	WOIb_HSize (ISP2_UpdateFlag=1, update)
B6	[2:0]	R_ISP_WOIb_VSize[10:8]	0x01	WOIb_VSize (ISP2_UpdateFlag=1, update)
B7	[7:0]	R_ISP_WOIb_VSize[7:0]	0xE0	WOIb_VSize (ISP2_UpdateFlag=1, update)
B8	[2:0]	R_ISP_WOIb_HOffset[10:8]	0x00	(ISP2_UpdateFlag=1, update)
B9	[7:0]	R_ISP_WOIb_HOffset[7:0]	0x00	(ISP2_UpdateFlag=1, update)
BA	[2:0]	R_ISP_WOIb_VOffset[10:8]	0x00	(ISP2_UpdateFlag=1, update)
BB	[7:0]	R_ISP_WOIb_VOffset[7:0]	0x00	(ISP2_UpdateFlag=1, update)
C0	[0]	UV_Swap	0x00	U V Swap
	[1]	YC_Swap	0x00	Y C Swap

	[3:2]	RGB565_mode[1:0]	0x00	RGB565_mode
	[4]	RGB565_En	0x00	RGB565 Enable (ISP2_UpdateFlag=1, update)
	[5]	RGB555_En	0x00	RGB555 Enable (ISP2_UpdateFlag=1, update)
	[6]	RGB444_En	0x00	RGB444 Enable (ISP2_UpdateFlag=1, update)
C1	[0]	Vsync_INV	0x00	Vsync inverse
	[1]	Hsync_INV	0x00	Hsync inverse
E3 - EE	[7:0]	Reserved	xx	Reserved

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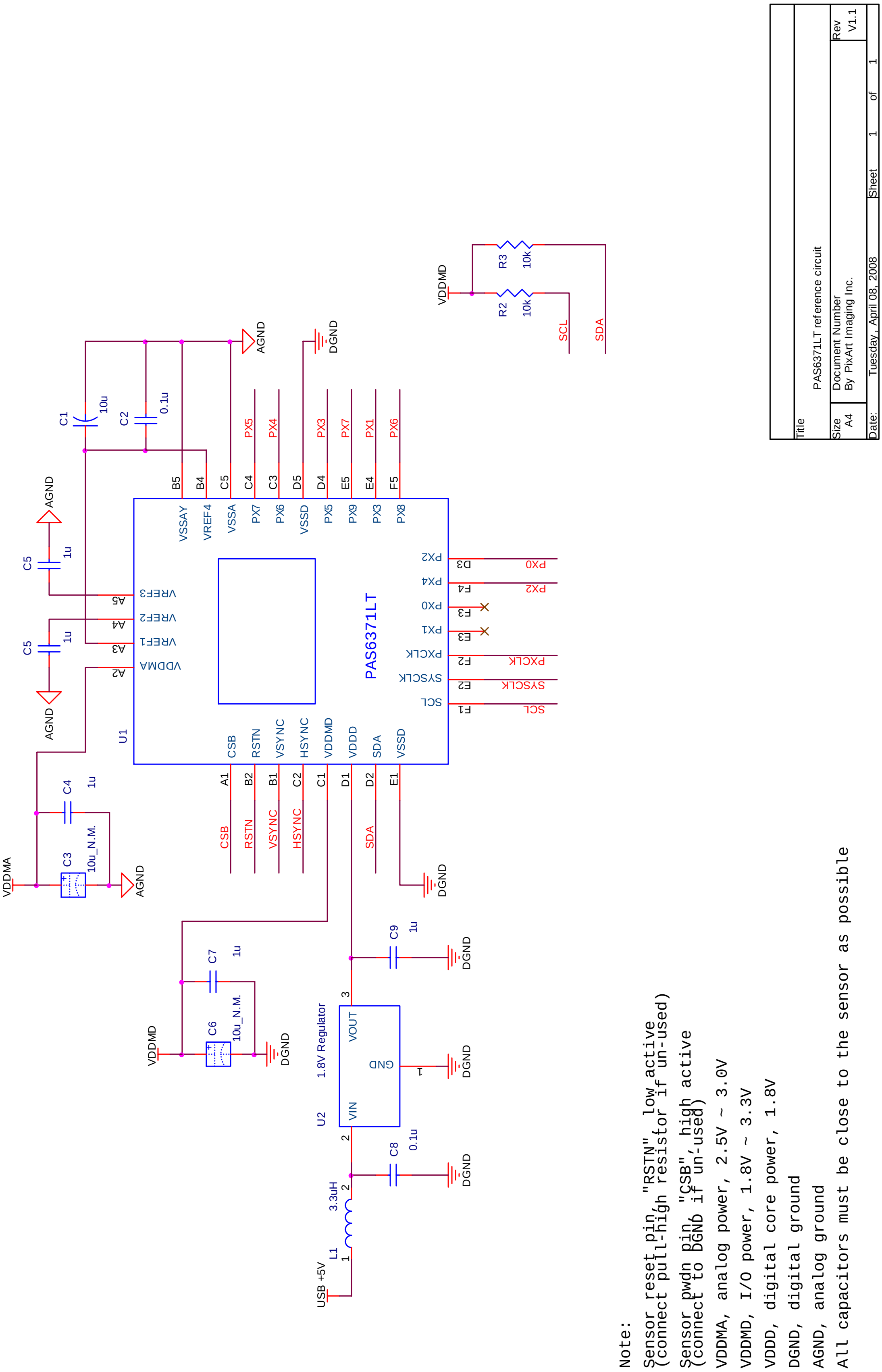
6. Reference Circuit Schematic



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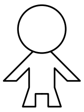
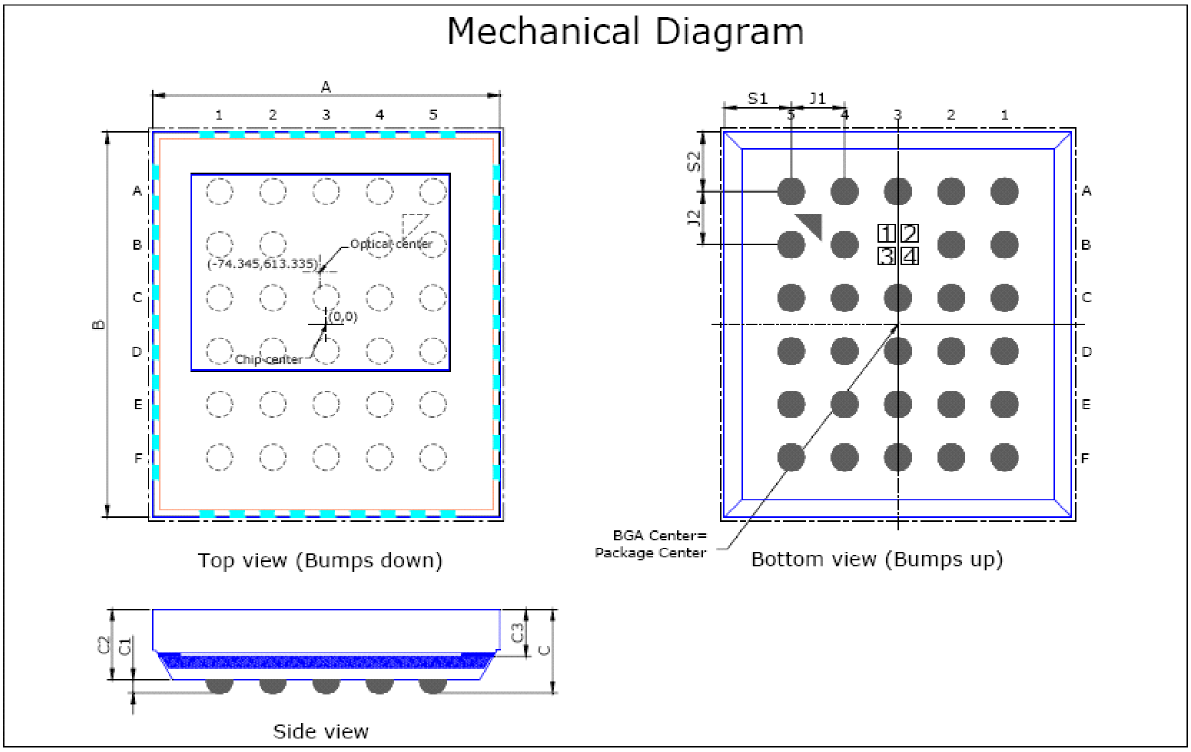
7. Package Information

	Symbol	Nominal	Min.	Max.
			μm	
Package Body Dimension X	**A**	4035	4010	4060
Package Body Dimension Y	**B**	4490	4465	4515
Package Height	**C**	985	925	1045
Ball Height	**C1**	160	130	190
Package Body Thickness	**C2**	825	780	870
Thickness of Glass surface to	**C3**	545	525	565
Ball Diameter	**D**	300	270	330
Total Pin Count	**N**	29		
Pin Count X axis	**N1**	5		
Pin Count Y axis	**N2**	6		
Pins Pitch X axis	**J1**	620		
Pins Pitch Y axis	**J2**	620		
Edge to Pin Center Distance along	**S1**	778	748	808
Edge to Pin Center Distance along	**S2**	695	665	725

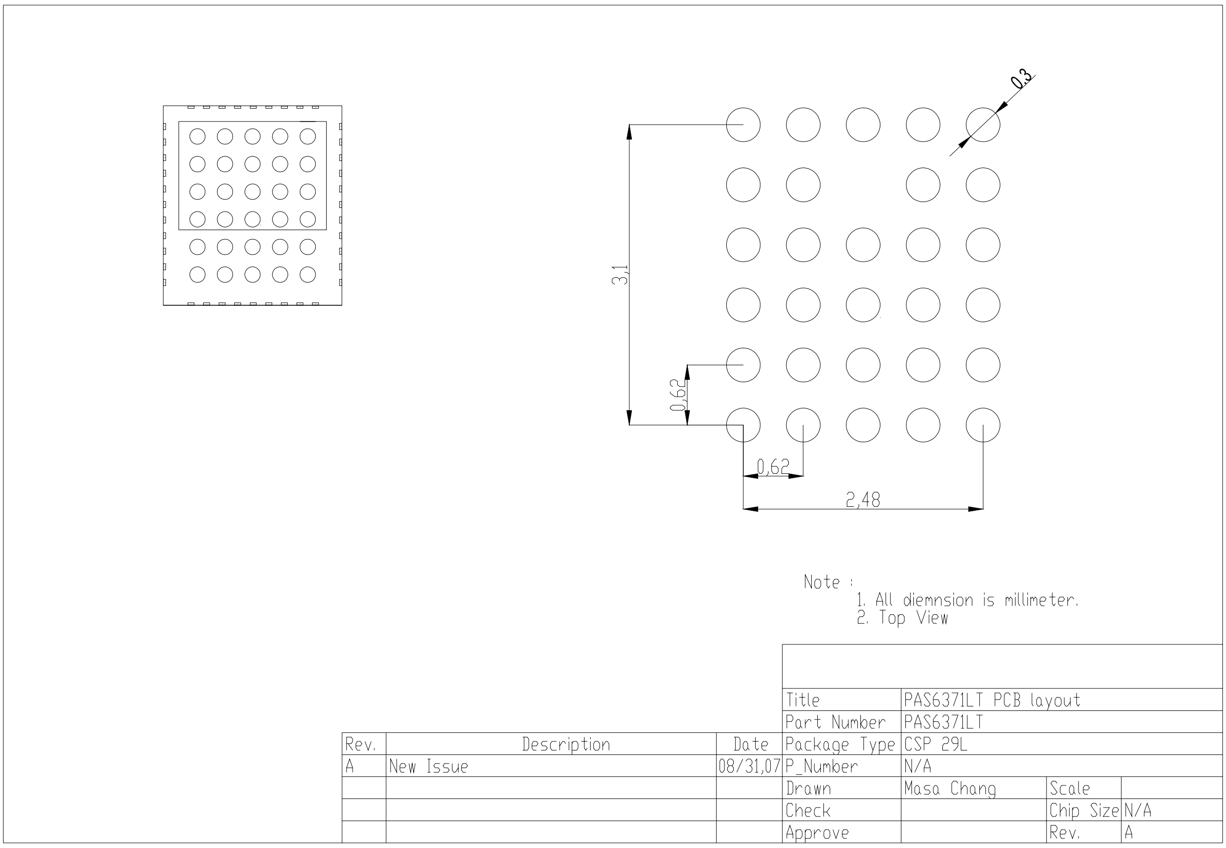

*Note



*Note:

The formation of image is the result formed by package Top view(A1 : left-up) and general Lens(invert and mirror the image).

Recommended Layout PCB

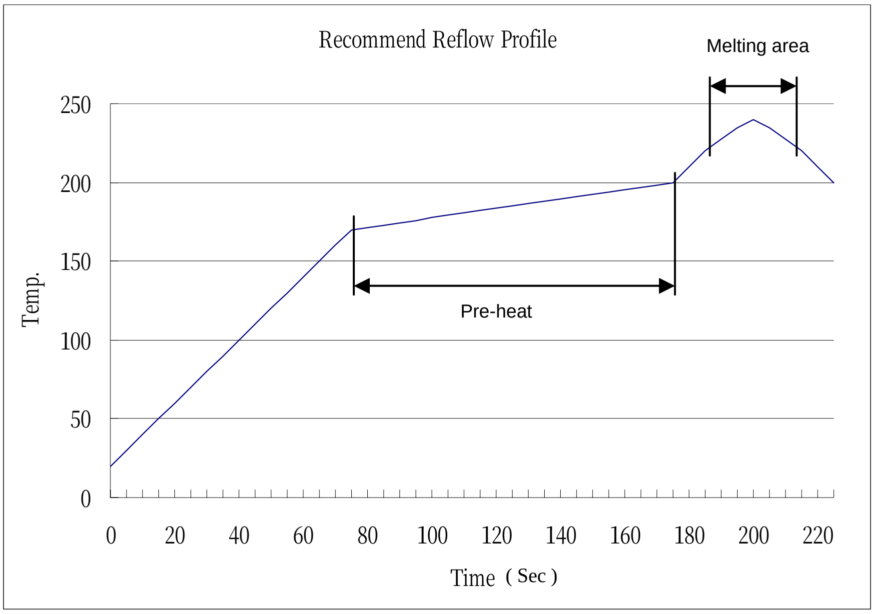


Recommended Condition For Infrared Reflow

Carefully observe the mounting conditions, recommended temperature profile when Mounting infrared reflows is show in the figure below.

After mounting on the mother board, it must be dispense epoxy in side of the CSP package.

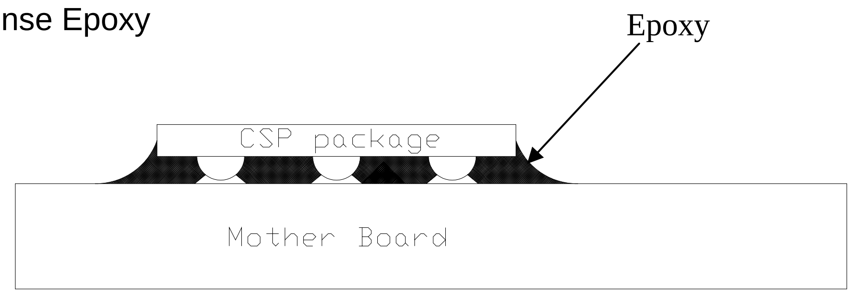
⊙ Reflow Profile



Recommend Pb-free solder paste vender & type : 1. Almit LFM-48W TM-HP
2. Senju M705-GRN360-K

Programming rate 1.5~2.5 ^{o}C/sec	⇨	Pre-heat 170~200^{o}C 90 +/- 30 sec	⇨	Melting area >220^{o}C 30~50sec with peak temperature 230~245^{o}C

⊙ Dispense Epoxy



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